REMARKS

This case has been carefully reviewed and analyzed in view of the Official Action dated 16 Sep. 2005.

Responsive to the rejections made in the Official Action, Claim 1 has been amended to clarify the combination of elements from a limitation of Claim 3 and Claim 3 has been re-written in independent form.

In the Official Action, Claim 1 is rejected under 35 U.S.C. 112(b) as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker (USPN 5402427, briefed as Parker). The Examiner states that Parker teaches test connectors that connect a circuit tester to an electronic device to be tested, but the objective of the pre-stored digital word generator provided by the claimed invention (refer to summary) is to produce multiple digital words, to reduce the cost and to make easy to program the digital word generator. More particularly (refer to field of the invention), the generator of the claimed invention employs an edge RAM for storing the preset information of TG data so as to provide multiple digital words, that is substantially different rather than Parker has tought.

Furthermore, the Claim 1 of the claimed invention is novel and non-obvious since it depicts that the pre-stored digital word generator comprises an edge memory (used to store a primary preset information), an edge address counter (electrically connected with the edge memory and used to point to an address of the edge memory), a reloadable down counter (electrically connected with the edge memory for accessing the primary preset information of the address) and a plurality of word generating circuits (electrically connected with the edge memory and the reloadable down counter).

As the Examiner admits, Parker doesn't explicitly teach a separate edge address counter and a reloadable down counter as stated in the present claimed invention, but Parker teaches the sequence controller for controlling the sequence directory and the like.

From above discussion, therefore, for overcoming the Examiner's rejection under 103, Claim 1 has been amended to include the limitation in Claim 3. The amended Claim

1 has non-obviousness since the word generating circuits further have the limitations of a rise register, a fall register, a rising comparator, a falling comparator and a latch component. Claims 3-7 have been amended to correct the dependencies to Claim 1.

Therefore, it is now believed that the subject Patent Application has been placed in condition for allowance and such action is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (703) 837-9600 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 04-0753. Please credit any overpayment to deposit Account No. 04-0753. A duplicate copy of this sheet is enclosed.

Dated: December 15, 2005

Respectfully submitted,

By _____
David E. Dougherty
Registration No.: 19,576
DENNISON, SCHULTZ, DOUGHERTY & MACDONALD
1727 King Street, Suite 105
Alexandria, VA 22314
(703) 837-9600
Attorneys for Applicant